STMicroelectronics
ADG - ASD & IPAD™ Division[1]
BU Rectifiers and Thyristors/Triacs

(1) ADG: Automotive and Discretes Group - ASD: Application Specific Device – IPAD™: Integrated Passive and Active Devices

PCN
Product/Process Change Notification

Qualification of a new assembly line in China for ST's Signal Schottky and DIACs housed in DO-35, MELF and MiniMelf packages

Notification number:	ADG-DIS/17/10070	**Issue Date**	17/01/2017
Issued by	Aline AUGIS		

Product series affected by the change

Signal Schottky Diodes

1Nxxx
BATxxx
TMMBATxxx
TMM6263FILM
TMBYV10-xxx
TMBATxxx

DIACS

DB3xxx
DB4xxx
TMMDB3xxx

Specific devices not expressly listed in the above table are included in this change.

Type of change

Back end realization

Description of the change

ST qualified a new assembly and test plant qualification in China.
The new production line will use similar equipment with same assembly and test flows and processes as on current production line.

Package	Current	New
DO-35	China 1	China 1 + China 2
MELF / MiniMELF		

Reason for change

This new plant will offer the possibility of expanding our **manufacturing capacity** on the considered products.

Former versus changed product:	The changed products do not present modified electrical, dimensional or thermal parameters, leaving unchanged the current information published in the product datasheet.

	The footprint recommended by ST remains the same. There is no change in the packing modes and the standard delivery quantities either.

Disposition of former products

The current source will continue the production in parallel, former products can still be used.

Marking and traceability

The traceability of products issued from the new assembly plant will be ensured by an **internal codification** and by the **Q.A. number**.

Qualification complete date	Week 15-2017

Forecasted sample availability

Product family	Sub-family	Commercial part Number	Availability date
Signal Schottky Diodes	DO-35	1N5711	Week 47-16
Signal Schottky Diodes	DO-35	BAT42	Week 47-16
Signal Schottky Diodes	DO-35	BAT48	Week 47-16
Signal Schottky Diodes	MELF	TMBYV10-40FILM	Week 47-16
Signal Schottky Diodes	MiniMELF	TMMBAT48FILM	Week 47-16
DIACs	DO-35	DB3 DB3TG	Week 04-17
DIACs	MiniMELF	TMMDB3	Week 14-17

Other part numbers will be available 6 weeks upon customer request

Change implementation schedule

Sales types	Estimated production start	Estimated first shipments
Signal Schottky	From week 44-2016	From week 16-2017
DIACs	From week 06-2017	From week 16-2017

Comments:	

Customer's feedback

Please contact your local ST sales representative or quality contact for requests concerning this change notification.
Absence of acknowledgement of this PCN within 30 days of receipt will constitute acceptance of the change
Absence of additional response within 90 days of receipt of this PCN will constitute acceptance of the change

Qualification program and results	QRP16075 Attached

Reliability Evaluation Report
Qualification of new subcontractor in China for Axial and Glass packages – Signal Schottky & Diacs products

General Information	
Product Line	*Rectifiers* *Diacs*
Product Description	*Signal Schottky* *Diacs*
Product perimeter	*BATxxx / 1Nxxx* *TMBYVxxFILM / TMBATxxFILM* *TMMxxxFILM* *DB3* *DB4* *TMMDB3*
Product Group	*ADG*
Product division	*ASD & IPAD*
Package	*MiniMELF* *MELF* *DO-35*
Maturity level step	*Under qualification*

Locations	
Wafer fab	*ST TOURS - FRANCE*
Assembly plant	*SUBCONTRACTOR – CHINA (9954)*
Reliability Lab	*ST TOURS - FRANCE*
Reliability assessment	PASS

DOCUMENT INFORMATION

Version	Date	Pages	Prepared by	Approved by	Comments
1.0	11-Aug-2016	8	Isabelle BALLON	Julien Michelon	Package Design Acceptance for Rectifiers perimeter
2.0	10-Jan-2017	11	Mickaël ALCANTARA	Julien Michelon	Package Design Acceptance for Diacs perimeter

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1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
JESD47	Stress-Test-Driven Qualification of Integrated Circuits
JESD 94	Application specific qualification using knowledge based test methodology
JESD 22	Reliability test methods for packaged devices

2 GLOSSARY

SS	Sample Size
BOM	Bill Of Material
HTRB	High Temperature Reverse Bias
TC	Temperature Cycling
THB	Temperature Humidity Bias
UHAST	Unbiased Humidity Accelerated Test
PCT	Pressure Cooker Test (Autoclave)
RSH	Resistance to Soldering Heat
SD	Solderability
GD	Generic Data
PC	Pre-conditioning (before test)
DPA	Destructive Physical Analysis

3 RELIABILITY EVALUATION OVERVIEW

3.1 Objectives

The objective of this report is to qualify a new subcontractor in China for the Axial Glass Diodes portfolio packaging, involving small Signal Schottky Rectifiers and Diacs.

The involved products are listed in table here below:

Commercial Product	Product description
BATxxx / 1Nxxx	Signal Schottky – DO-35 package
TMBYVxxxFILM / TMBATxxFILM	Signal Schottky – MELF package
TMMxxxFILM	Signal Schottky – MiniMELF package
DB3	Diac – DO-35 package
DB4	Diac – DO-35 package
TMMDB3	Diac – MINIMELF

The reliability test methodology used follows the JESD47-H: « Stress Test Driven Qualification Methodology ».
The following reliability tests ensuing are:

- TC and IOLT to ensure the mechanical robustness of the products.
- HTRB to evaluate the risk of contamination from the resin and the assembly process versus the die layout sensitivity.
- THB, uHAST to check the robustness to corrosion and the good package hermeticity
- RSH, solderability to check that package can be soldered on board
- Whiskers to check leadfinishing quality

3.2 Conclusion

Qualification Plan requirements have been fulfilled without exception. Reliability tests have shown that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests demonstrates the robustness of the products and safe operation, which is consequently expected during their lifetime.

4 DEVICE CHARACTERISTICS

4.1 Device description

Refer to products datasheets.

DO-35

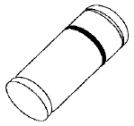
4.2 Construction Note

	BATxxx / 1Nxxxx
Wafer/Die fab. information	
Wafer fab manufacturing location	ST Tours (France)
Technology / Process family	Signal SCHOTTKY
Wafer Testing (EWS) information	
Electrical testing manufacturing location	ST Tours (France)
Assembly information	
Assembly site	Subcontractor in CHINA *(9954)*
Package description	DO-35
Molding compound	ECOPACK®2 compliant component
Lead finishing/bump solder material	Pure Tin
Final testing information	
Testing location	Subcontractor in CHINA *(9954)*

	DB3 / DB4
Wafer/Die fab. information	
Wafer fab manufacturing location	ST Tours (France)
Technology / Process family	DIAC
Wafer Testing (EWS) information	
Electrical testing manufacturing location	ST Tours (France)
Assembly information	
Assembly site	Subcontractor in CHINA *(9954)*
Package description	DO-35
Molding compound	ECOPACK®2 compliant component
Lead finishing/bump solder material	Pure Tin
Final testing information	
Testing location	Subcontractor in CHINA *(9954)*

4.3 Device description

Refer to products datasheets.



MINIMELF
(Glass)

4.4 Construction Note

	TMMxxxFILM
Wafer/Die fab. information	
Wafer fab manufacturing location	ST Tours (France)
Technology / Process family	Signal SCHOTTKY
Wafer Testing (EWS) information	
Electrical testing manufacturing location	ST Tours (France)
Assembly information	
Assembly site	Subcontractor in CHINA *(9954)*
Package description	MiniMELF
Molding compound	ECOPACK®2 compliant component
Lead finishing/bump solder material	Pure Tin
Final testing information	
Testing location	Subcontractor in CHINA *(9954)*

	TMMDB3
Wafer/Die fab. information	
Wafer fab manufacturing location	ST Tours (France)
Technology / Process family	DIAC
Wafer Testing (EWS) information	
Electrical testing manufacturing location	ST Tours (France)
Assembly information	
Assembly site	Subcontractor in CHINA *(9954)*
Package description	MiniMELF
Molding compound	ECOPACK®2 compliant component
Lead finishing/bump solder material	Pure Tin
Final testing information	
Testing location	Subcontractor in CHINA *(9954)*

4.5 Device description

Refer to products datasheets.

MELF
(glass)

4.6 Construction Note

	TMBYVxxFILM / TMBATxxFILM
Wafer/Die fab. information	
Wafer fab manufacturing location	ST Tours (France)
Technology / Process family	Signal SCHOTTKY
Wafer Testing (EWS) information	
Electrical testing manufacturing location	ST Tours (France)
Assembly information	
Assembly site	Subcontractor in CHINA *(9954)*
Package description	MELF
Molding compound	ECOPACK®2 compliant component
Lead finishing/bump solder material	Pure Tin
Final testing information	
Testing location	Subcontractor in CHINA *(9954)*

5 TESTS RESULTS SUMMARY

5.1 Test vehicle

Lot #	Commercial Product	Package	Comments
Lot 1	DB3	DO-35	Qualification lots (Diacs)
Lot 2	DB4	DO-35	
Lot 3	TMMDB3	MiniMELF	
Lot 4	BAT41	DO-35	Qualification lots (Rectifiers)
Lot 5	TMMBAT48FILM	MiniMELF	
Lot 6	TMBAT49FILM	MELF	

Detailed results in below chapter will refer to these references.

5.2 Test plan and results summary

Test	PC	Std ref.	Conditions	SS	Steps	Failure/SS					
						Lot 1	Lot 2	Lot 3	Lot 4	Lot 5	Lot 6
Die Oriented Tests											
HTRB	N	JESD22 A-108	Temperature = 125°C Tension VAC = 36V	77	1000 hours		0/77				
			Temperature = 125°C Tension VAC = 28V	154	1000 hours	0/77		0/77			
			Temperature = * Tension DC = 80V	194	1000 hours				0/40	0/77	0/77
Package Oriented Tests											
TC	N	JESD22 A-104	Frequency (cy/h) = 2cy/h Temperature (high) = 150°C Temperature (low) = -65°C	454	1000 cycles	0/100	0/100	0/100		0/77	0/77
RSH		JESD22 B-106 JESD22 A-111	DO35: 7s/270°C MELF/MiniMELF: 10s/260°C + visual inspection	90	-		0/30	0/30			0/30
SD	N	0018688	Dry ageing SnPb 220°C	20	-					0/10	0/10
			Wet ageing SnPb 220°C	20						0/10	0/10
			Dry ageing SnAgCu 245°C	20						0/10	0/10
			Wet ageing SnAgC 245°C	20						0/10	0/10
Lead Integrity	N	JESD22 B-105	Torsion test Uc (180° 2x)	5	-				0/5		
			Bending condition B (45°)	5					0/5		
			Tension condition A (8ounces/30s)	5					0/5		
			Fatigue condition C (3ounces)	5					0/5		
Gross Leak	N	JESD22 A-109	Bubble test	117	-	0/39			0/39		0/39
Whiskers	N	JESD201A (CLASS 1)	Pb free reflow TC -55°C/85°C 10 min	6	1500C	1 lot in MiniMELF: 0/6 1 lot in DO-35: 0/6					
			Pb free reflow THS 30°C/RH = 60%	6	4000h	1 lot in MiniMELF: 0/6 1 lot in DO-35: 0/6					
			Pb free reflow THS 55°C / RH = 85%	6	4000h	1 lot in MiniMELF: 0/6 1 lot in DO-35: 0/6					
			No reflow TC -55°C/85°C 10 min	6	1500C	1 lot in MiniMELF: 0/6 1 lot in DO-35: 0/6					
			No reflow THS 30°C / RH = 60%	6	4000h	1 lot in MiniMELF: 0/6 1 lot in DO-35: 0/6					
			No reflow THS 55°C / RH = 85%	6	4000h	1 lot in MiniMELF: 0/6 1 lot in DO-35: 0/6					
			SnPb reflow TC -55°C/85°C 10 min	6	1500C	1 lot in MiniMELF: 0/6 1 lot in DO-35: 0/6					
			SnPb reflow THS 30°C / RH = 60%	6	4000h	1 lot in MiniMELF: 0/6 1 lot in DO-35: 0/6					
			SnPb reflow THS 55°C / RH = 85%	6	4000h	1 lot in MiniMELF: 0/6 1 lot in DO-35: 0/6					

***** Lot 4: Ta = 125°C
Lot 5: Ta = 100°C
Lot 6: Ta = 80°C

6 ANNEXES

6.1 Tests description

Test name	Description	Purpose
Die-oriented		
HTRB High Temperature Reverse Bias	High Temperature Reverse Bias The device is stressed in static configuration, trying to satisfy as much as possible the following conditions: - low power dissipation - max. supply voltage compatible with diffusion process and internal circuitry limitations	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. To maximize the electrical field across either reverse-biased junctions or dielectric layers, in order to investigate the failure modes linked to mobile contamination, oxide ageing, layout sensitivity to surface effects.
Package-oriented		
TC Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
RSH Resistance to Solder Heat	Package is dipped by the leads 2 times in a solder bath.	To simulate wave soldering process and verify that package will not be thermally damaged during this step.
SD Solderability	Wet ageing + dipping in a solder bath. Assessment by visual inspection of the leads.	To ensure good wettability of the leads
Lead Integrity	Mechanical stresses on leads: Pull, twist, torque, bending	To check leads integrity and good behavior against handling-related mechanical stresses
Gross leak	For cavity packages.	To assess package hermeticity.
Whiskers	This test is intended to check Tin plated packages quality versus whiskers risk.	It is applicable for studying tin whisker growth from finishes containing a predominance of tin (Sn).

Public Products List

Publict Products are off the shelf products. They are not dedicated to specific customers, they are available through ST Sales team, or Distributors, and visible on ST.com

PCN Title : Qualification of a new assembly line in China for ST's Signal Schottky and DIACs housed in DO-35, MELF and MiniMelf packages

PCN Reference : ADG/17/10070

Subject : Public Products List

Dear Customer,

Please find below the Standard Public Products List impacted by the change.

DB3	DB4	BAT48
1N5822RL	TMBYV10-60FILM	BAT41
1N6263	TMBYV10-40FILM	1N5818
TMMDB3TG	TMMBAT46FILM	TMMBAT41FILM
1N5711	TMMBAT42FILM	TMMBAT43FILM
DB3TG	1N5819	TMMDB3
BAT46	TMBAT49FILM	1N5817
BAT43	1N5822	TMMBAT48FILM
BAT42	1N5819RL	

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